providing a plurality of logic gates each receiving data inputs and control signals, wherein each data input uses a single transistor;

connecting the logic gates using a plurality of shared data lines, wherein the plurality of shared data lines interface through a transistor on each of the logic gates to provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates; and

shifting data received at the data inputs by one or more data bits based upon the control signals and the connections of the shared data lines, wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines.

REMARKS

Applicant thanks the Examiner for the in-person interview held on January 10, 2003.

Claims 1-20 are pending. By this amendment, claims 1 and 11 are amended. No new matter is introduced. Support for the amendments may be found at least on page 4, lines 6-11 of the specification. Reconsideration and allowance of all pending claims is respectfully requested in view of the preceding amendments and following remarks.

Specification Objection

The specification is objected to because of certain informalities. The specification has been amended to change the term "multiplexor" to "multiplexer" as suggested by the Examiner. In addition, the title of the specification has been amended to clearly describe the invention to which the claims are directed. Withdrawal of the objection is respectfully requested.

Claim Rejections Under 35 U.S.C. §102

Claims 1-20 are rejected under 35 U.S.C. §102 (b) over U.S. Patent 5,553,010 to Tanihira et al. (hereafter Tanihira). This rejection is respectfully traversed.

Tanihira is directed to a data shifting circuit capable of an original data width rotation and a double data width rotation. However, Tanihira does not disclose or suggest "wherein each data input uses a single transistor ... the shared data lines interfacing through a transistor on each of the logic gates to provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates, ... wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines" as recited in amended claim 1. There is no indication or suggestion that the logic gates of Tanihira, i.e., Logic I 110-113 & 15, Logic II 120-123 & 16, Logic III 130-133 & 17, and Logic IV 140-143 & 18, use a single transistor

for each data input, i.e., Din 0, Din 1, Din2, and Din 3. Since Tanihira does not disclose or suggest all of the elements of amended claim 1, claim 1 is allowable over Tanihira.

Claims 2-10 are allowable because they depend from allowable claim 1 and for the additional features they recite.

Regarding claim 11, Tanihira does not disclose or suggest "wherein each data input uses a single transistor; ... wherein the plurality of shared data lines interface through a transistor on each of the logic gates to provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates; ... wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines" as recited in amended claim 11. As noted above, there is no indication or suggestion that the logic gates of Tanihira, i.e., Logic I 110-113 & 15, Logic II 120-123 & 16, Logic III 130-133 & 17, and Logic IV 140-143 & 18, use a single transistor for each data input, i.e., Din 0, Din 1, Din2, and Din 3. Since Tanihira does not disclose or suggest all of the elements of amended claim 11, claim 11 is allowable over Tanihira.

Claims 12-20 are allowable because they depend from allowable claim 11 and for the additional features they recite. Withdrawal of the rejection of claims 1-20 under 35 U.S.C. §102 (b) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 8 and 18 are rejected under 35 U.S.C. §103 (a) over Tanihira in view of U.S. Patent 5,822,231 to Wong et al. (hereafter Wong). This rejection is respectfully traversed.

Claims 8 and 18 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 8 and 18 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above amendments and remarks, Applicant respectfully requests reconsideration and allowance of all pending claims.

The Commissioner is hereby authorized to charge or credit any deficiencies in connection with this amendment to deposit account 08-2025.

Attached hereto are a marked-up version of the changes made to the specification and claims by the current amendment, and a clean version of all pending claims. The attached pages are captioned "**Version with markings to show changes made**", and "**Pending Claims**" respectively.

Respectfully Submitted,

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John K. Harrop,
Registration No. 41,817
DORSEY & WHITNEY LLP
1001 Pennsylvania Ave, N.W.
Suite 400 South
Washington, DC 20004
Tel. (202) 442-3524
Fax (202) 442-3199

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

Title of the specification has been amended as follows:

APPARATUS AND METHOD FOR SHARING DATA FET FOR A FOUR-WAY MULTIPLEX[O]ER

IN THE SPECIFICATION:

Paragraph beginning at page 2, line 4, has been amended as follows:

The present invention relates to a [multiplexor] multiplexer for shifting data.

Paragraphs beginning at page 2, line 13, have been amended as follows:

FMAC operations are implemented in multiple stages, and the final stage is used to normalize the value of the mantissa of the result. In particular, according to use of floating point numbers complying with the IEEE standard, the result is shifted to obtain a leading one in the mantissa and thus remove all leading zeros. This produces a normalized result for the FMAC operation. To obtain a leading one in the result, [multiplexors] multiplexers are typically used in order to shift the result until the value one resides in the most significant bit position.

[Multiplexors] Multiplexers are known in the art and use control signals in order to shift input data among output lines based upon the control signals. [Multiplexor] Multiplexers can require many inputs for the data lines and the control signals, and each data input can require a separate data line and individual transistor for interfacing the data line with a corresponding logic gate that performs the data shifting. Due to the high number of inputs, individual data lines increase the number of transistors required for each gate, thus increasing the area and power consumption of each gate.

Accordingly, a need exists for a [multiplexor] multiplexer for data shifting having reduced area and potentially other advantages.

Paragraphs beginning at page 3, line 7, has been amended as follows:

A logic circuit consistent with the present invention uses data sharing in a [multiplexor] multiplexer for shifting data. It includes a plurality of logic gates and a plurality of shared data lines connecting the logic gates. Each logic gate receives data inputs and control signals, and the shared data lines provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates. In operation, the logic gates shift data received at the data inputs based upon the control signals and the connections of the shared data lines to produce a shifted data output.

A method consistent with the present invention includes sharing data among logic gates in a [multiplexor] multiplexer for shifting data. It includes providing a plurality of logic gates each receiving data inputs and control signals, and connecting the logic gates using a plurality of shared data lines. The data lines provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates. Data received at the data inputs is shifted based upon the control signals and the connections of the shared data lines to produce a shifted data output.

Paragraph beginning at page 4, line 1, has been amended as follows:

FIG. 1 is a block diagram of a portion of a [multiplexor] multiplexer illustrating data sharing consistent with the present invention; and

Paragraphs beginning at page 4, line 6, have been amended as follows:

A [multiplexor] multiplexer consistent with the present invention uses data sharing among field-effect transistors (FETs) in order to reduce the number of transistors required by each logic gate. Therefore, instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines.

FIG. 1 is a block diagram of a portion 10 of a [multiplexor] multiplexer for implementing data sharing consistent with the present invention. This example only illustrates four logic gates among many logic gates that may be required to implement a particular [multiplexor] multiplexer depending upon the size of a data bus involved. This example illustrates four logic gates 11, 12, 13, and 14. Each logic gate receives data inputs, and produces shifted data outputs based upon input control signals and how the data is shared among the logic gates as determined by connections of shared data lines.

Paragraph beginning at page 5, line 3, has been amended as follows:

The shifted data output 16, 19, 22, and 25 may include a plurality of data outputs for each logic gate 11-14. For example, this implementation may be used for dual rail Domino CMOS logic, which produces two outputs for each logic gate, a high output and a complementary low output. Other types of logic gates may likewise implement the data sharing in a [multiplexor] multiplexer.

Paragraph beginning at page 10, line 18, has been amended as follows:

Accordingly, use of data sharing consistent with the present invention provides for the elimination of transistors within each logic gate and a savings in area and power consumption on an integrated circuit chip implementing the logic gates. Although two stages of shifting have been shown, different numbers of stages may be used. The number of stages and use of

a [multiplexor] multiplexer using logic circuit 10 may depend upon a particular application, and performing an FMAC operation is only one such example.

Paragraph beginning at page 16, line 1, has been amended as follows:

Data sharing among adjacent logic gates for shifting data in a [multiplexor] multiplexer. Each logic gate implements two stages of shifting and provides for data sharing by connecting data inputs among the logic gates. Based upon the data sharing connections, control signals feed bits into each logic gate from adjacent logic gates to perform various shifting operations on a data bus.

IN THE CLAIMS:

Claims 1 and 11 have been amended as follows:

1. (Amended) A logic circuit for use in a [multiplexor] multiplexer to shift data, comprising:

a plurality of logic gates, each logic gate receiving data inputs and control signals, wherein each data input uses a single transistor; and

a plurality of shared data lines connecting the logic gates, the shared data lines interfacing through a transistor on each of the logic gates to provide [providing] a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates,

wherein the logic gates shift data received at the data inputs by one or more data bits based upon the control signals and the connections of the shared data lines, and wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines.

11. (Amended) A method of using a [multiplexor] multiplexer to shift data, comprising:

providing a plurality of logic gates each receiving data inputs and control signals, wherein each data input uses a single transistor;

connecting the logic gates using a plurality of shared data lines, wherein the plurality of shared data lines interface through a transistor on each of the logic gates to provide [providing] a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates; and

shifting data received at the data inputs by one or more data bits based upon the control signals and the connections of the shared data lines, wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines.